AMENDMENTS TO THE CLAIMS

Claims 1 – 36. (canceled)

37. (currently amended) A method of reading a resistive memory device comprising a plurality of ~~stacked layers~~ memory slices of resistive memory cells, each ~~layer~~ slice comprising an array of memory cells arranged in rows and columns and having an associated access transistor, said method comprising:

decoding a selected memory cell address as a column select signal, a row select signal, and a layer select signal;

using said layer select signal to select one of said layers for a read operation;

using said row select signal to select a row of memory cells of said selected one layer; and

using said column select signal to select ~~the~~ a same column of memory cells in each of said layers by turning on ~~an~~ said access ~~transistors~~ transistor coupled to said same ~~columns~~ column.

38. (original) A method as in claim 37, wherein said resistive memory cells are MRAM memory cells.

39. (original) A method as in claim 38 further comprising sensing a resistance value of a selected memory cell with a sense amplifier coupled to said access transistor.

Claims 40 – 61. (canceled)

62. (new) A method of reading a resistive memory device comprising a plurality of memory slices of resistive memory cells, each memory slice comprising an array of memory cells arranged in rows and columns, said method comprising:

identifying a selected memory cell in said resistive memory device;

addressing said selected memory cell in said resistive memory device;

enabling an access gate corresponding to a memory slice including the selected memory cell;

coupling said memory cell to an input of a sense amplifier; and

coupling a reference line to a second input of said sense amplifier.

63. (new) The method of said 62, wherein said access gate is a transistor.

64. (new) The method of said 62, wherein said identifying comprises a determination of said memory slice containing the selected memory cell.

65. (new) The method of said 62, wherein said identifying comprises a determination of a row, column and array layer of the selected memory cell.

66. (new) The method of said 62, further comprising the step of determining the logic of said selected memory cell.

67. (new) The method of said 66, wherein said determining the logic step comprises sensing a logic state of said selected memory cell.

68. (new) The method of said 62, wherein said coupling said memory cell comprises:

coupling said selected memory cell to a sense line associated with said selected memory cell.

69. (new) The method of said 68, wherein said coupling said memory cell further comprises:

coupling said sense line to an associated sense line interconnect.

70. (new) The method of said 69, wherein said coupling said memory cell further comprises:

coupling said sense line interconnect to said access gate.

71. (new) The method of said 70, wherein said coupling said memory cell further comprises:

coupling said access gate to an associated bit line.

72. (new) The method of said 71, wherein said coupling said memory cell further comprises:

coupling said bit line to said input of said sense amplifier.

73. (new) A method of reading a resistive memory device comprising a plurality of memory slices of MRAM memory cells, each memory slice comprising an array of memory cells arranged in rows and columns and having an associated access transistor, said method comprising:

decoding a selected memory cell address as a column select signal, a row select signal, and a layer select signal;

enabling a read/write row line associated with said selected memory cell in one of said plurality of memory slices;

coupling a sense line with said selected memory cell; and

determining a logic state of said selected memory cell.

74. (new) The method of said 73, wherein said determining said logic state comprises sensing a resistance of said selected memory cell.

75. (new) The method of said 73, said sensing said logic state comprises sensing magnetic moments of said selected memory cell.